a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

2.(Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface in a decoder circuit of a peripheral [circuitry] circuit of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

3.(Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface in a buffer circuit of a peripheral [circuitry] circuit of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

4.(Amended) An electro-optical device comprising:

[an active matrix circuit provided on an insulating surface;]

at least two transistors provided on [said] an insulating surface in a decoder circuit of a peripheral [circuitry] circuit of said electro-optical device [provided around said active matrix circuit];

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are provided in a common island.

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

B1 cont.

5.(Amended) An electro-optical device comprising:

[an active matrix circuit provided on an insulating surface;]

at least two transistors provided on [said] an insulating surface in a buffer circuit of a peripheral [circuitry] circuit of said electro-optical device [provided around said active matrix circuit];

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are provided in a common island.

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

6.(Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,]

wherein [said] channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively[, and].

[wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

7.(Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,]

wherein [said] channel-forming regions of said at least two transistors are provided in a common island[; and].

[wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

8.(Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface in a peripheral [circuitry] circuit of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,]

wherein [said] channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively[, and].

[wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

9.(Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface in a peripheral [circuitry] circuit of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

[wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,]

wherein [said] channel-forming regions of said at least two transistors are provided in a common island[; and].

[wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.]

10.(Amended) An electro-optical device comprising: [which employs a thin-film semiconductor which is formed on an insulating surface, wherein

the thin-film semiconductor has a region which can be regarded as being effectively monocrystalline,

the region contains carbon and nitrogen atoms at a concentration of 5×10^{18} cm^{-3} or less, oxygen atoms at a concentration of 5×10^{19} cm^{-3} or less, and

wherein the region constitutes at least part of a channel-forming region.]

at least two transistors provided on an insulating surface in a XY-branching circuit of a peripheral circuit of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

B1 Cont.

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are provided in a common island.

B2

38.(Amended) The device of claim [1] 58 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

39.(Amended) The device of claim [1] 58 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

40.(Amended) The device of claim [2] 59 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

41.(Amended) The device of claim [2] 59 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

42.(Amended) The device of claim [3] 60 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and

a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

43.(Amended) The device of claim [3] 60 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

44.(Amended) The device of claim [4] 61 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

45.(Amended) The device of claim [4] 61 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

46.(Amended) The device of claim [5] 62 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

47.(Amended) The device of claim [5] 62 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

48.(Amended) The device of claim [6] 63 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and

a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

49.(Amended) The device of claim [6] 63 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

50.(Amended) The device of claim [7] 64 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

51.(Amended) The device of claim [7] 64 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

B2 cont.

52.(Amended) The device of claim [8] 65 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

53.(Amended) The device of claim [8] 65 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

54.(Amended) The device of claim [9] 66 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and

a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

55.(Amended) The device of claim [9] 66 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

56.(Amended) The device of claim [10] 67 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

57.(Amended) The device of claim [10] 67 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

Please add new claims 58-70 as follows.

58. The device of claim 1 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

59. The device of claim 2 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

60. The device of claim 3 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

61. The device of claim 4 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

62. The device of claim 5 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

B3 Cont.

63. The device of claim 6 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

64. The device of claim 7 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

65. The device of claim 8 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

66. The device of claim 9 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

67. The device of claim 10 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

B3 Cont.

68. The device of claim 10 wherein said electro-optical device has a memory.

69. The device of claim 10 wherein said electro-optical device has a decoder.

70. The device of claim 10 wherein said electro-optical device is a display system.

Add D7

REMARKS

The Official Action dated December 27, 2000 has been received and its contents carefully noted. Claims 1-57 were pending in the present invention prior to the above amendment. Claims 1-10 and 38-57 have been amended herewith, claims 15 and 21 have been canceled and new claims 58-70 have been added to recite additional protection to which Applicants are entitled. Accordingly, claims 1-14, 16-20 and 22-70 are pending in the subject application and, for the reasons set forth in detail below, are now believed to be in condition for allowance.